hxISDE™ HyperX Integrated Software Development Environment

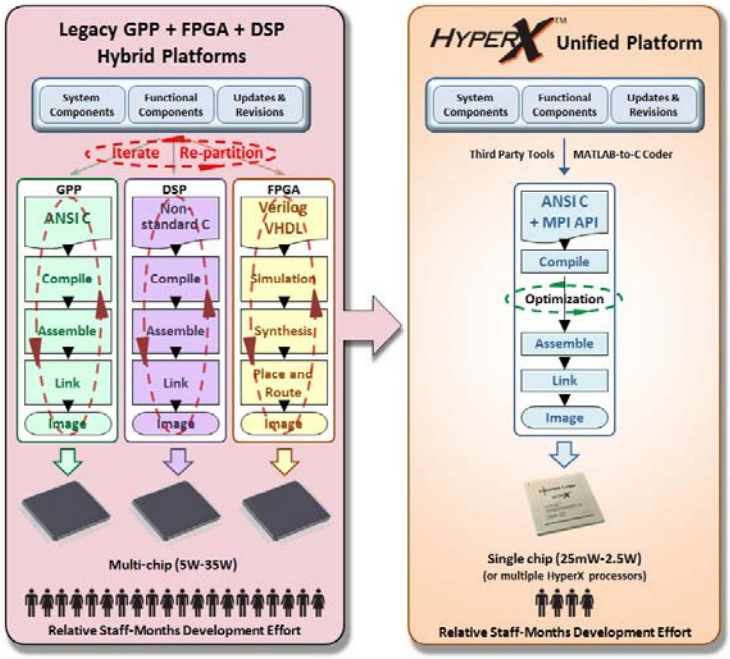
HyperX™ Technology – Rapid Development of Low Power, Many-Core Systems

HyperX Tools – Unlocking the True Potential for Many-Core Architectures

HyperX technology combines the standards-based programming ease of general purpose processors (GPPs) and the high computational performance of traditional DSPs and FPGAs into a low power, real-time adaptable processing fabric. The HyperX™ hx3100 processor is comprised of an array of 100 DSP/GPP processing elements (PEs) interconnected with a memory and communication network to speed autonomous data movement across the chip. The hxISDE tool suite and HyperX processor have been designed together to achieve far lower power and far shorter design time than conventional multi-chip processing solutions.

This low risk, field-proven solution brings:

- ✓ Increased revenue from first-to-market advantage
- ✓ Massive increase in productivity
- ✓ Lower development cost
- ✓ High portability with standard ANSI C
- ✓ Scalability to multi-device systems with a single ISDE



hxISDE speeds many-core development

Most high performance embedded systems have traditionally required a combination of FPGAs, DSPs, GPPs, and/or hardware accelerators. This hybrid solution is plagued with ever lengthening design and verification cycles due to its combination of multiple tool flows, inconsistent programming languages, RTL synthesis, place and route, and non-portable IP. Debugging the system is extremely difficult because a different environment is used for each device type.

"HyperX and FPGA development efforts within our company indicate a 5X productivity improvement when developing for the HyperX."

- a Fortune 100 Defense Company

In contrast, the HyperX ISDE (hxISDE) tool suite speeds application development from an initial ANSI C based prototype to a full speed specification-compliant system in an incremental series of steps, without resorting to complex heterogeneous processors, or expensive custom accelerator design. This robust, feature rich platform lets the user define the entire system in a hierarchical C-based model using an API based on the open industry-standard Message Passing Interface (MPI). This approach facilitates the natural separation of algorithms into distinct components. The industry-proven MPI has been enhanced to deliver the low-latency, high-throughput data transfer capabilities required for DSP and image processing.

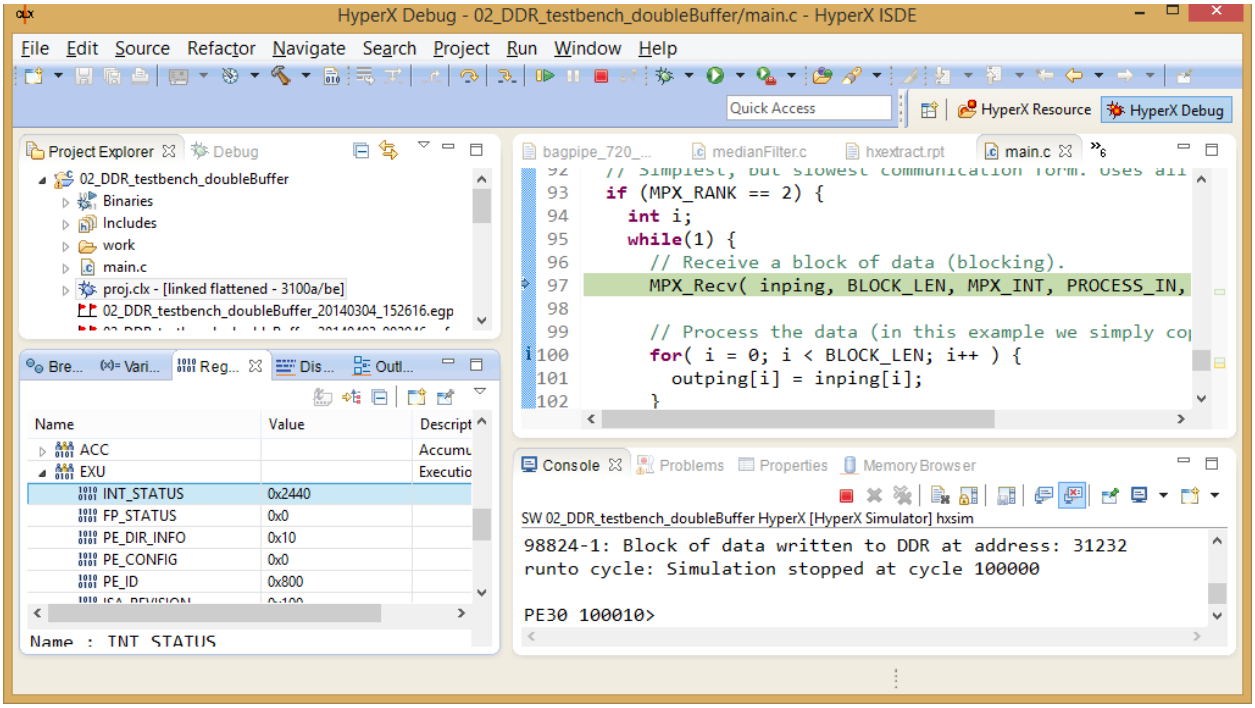
High productivity with automation and control

The HyperX tool suite takes user-specified constraints and MPI communication information between different components, and then optimizes the mapping for the best performance and resource utilization. The complete library of synchronization and communication utilities makes it easy to realize the full potential of HyperX many-core technology.

This automation does not force the advanced user to give up control. Rather, this comprehensive set of tools has been refined with years of use in the relevant application domains, and they allow direct manual control over communication, optimization, and mapping options when desired. Users are free to use a different level of abstraction in different parts of the design. One part can include optimized code and detailed physical mapping information that remains fixed, while other parts of the design rely on the automatically generated mapping.

Familiar Eclipse CDT based tool flow

The hxISDE is based on the popular Eclipse graphical development environment. The hxISDE serves as the center of the software development tool chain, from compiling the first C files all the way to real time analysis of the application running in the HyperX Hardware Application Development System (hxHADS). New capabilities and features have been added to help the user best utilize the network of parallel cores in the HyperX device.



hxISDE supports C based design and debug

Source code entry and project management

The C-code editor includes complete color coding, language feature recognition, tips for expression detail, and standard productivity features. The source editor is linked with other tools to provide a multi-context capability for single stepping and breakpoint control. The project explorer displays all source and header files, as well as an outline view that shows all variables.

C compiler tool chain

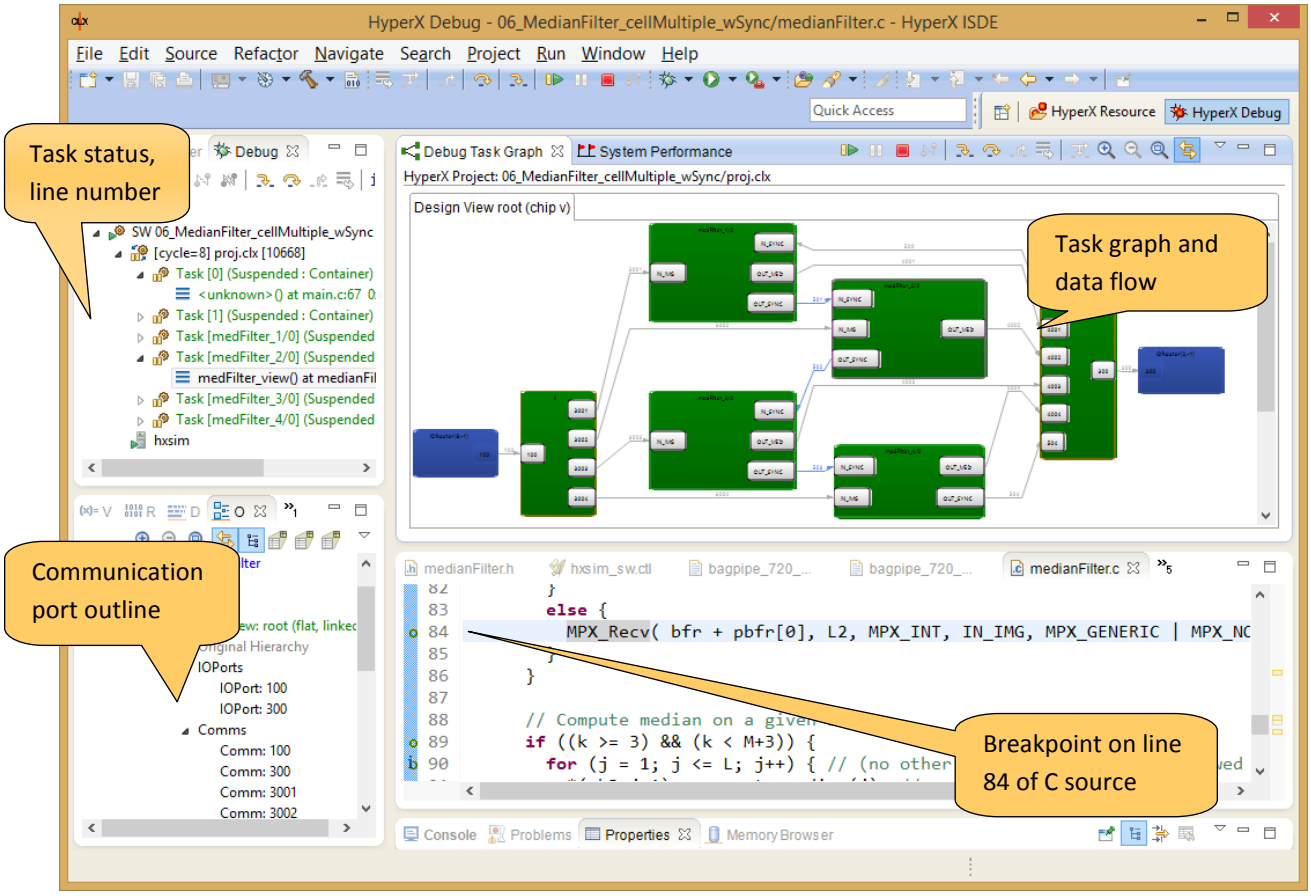
This state of the art compiler minimizes the amount of assembly language entry normally required in high performance applications. The HyperX compiler supports integer and floating data types, as well as extended precision integer operations. It supports a variety of optimization options that trade off performance, area, and ease of debug visibility. It compiles tight C loops into optimized assembly code that makes the most of the processors' zero-overhead looping and branching capabilities.

The compiler and linker support hierarchical design, incremental compilation, and the reuse of IP components. The tool chain also supports the cell construct to group the code doing the processing work (the tasks) and the communication ports (which pass data to other tasks.) The cell can be re-used hierarchically, and the connections between cell ports are preserved over different optimizations or changes. This higher level of abstraction frees the user from having to specify absolute physical routing information, raising design productivity.

Message Passing Interface API and support

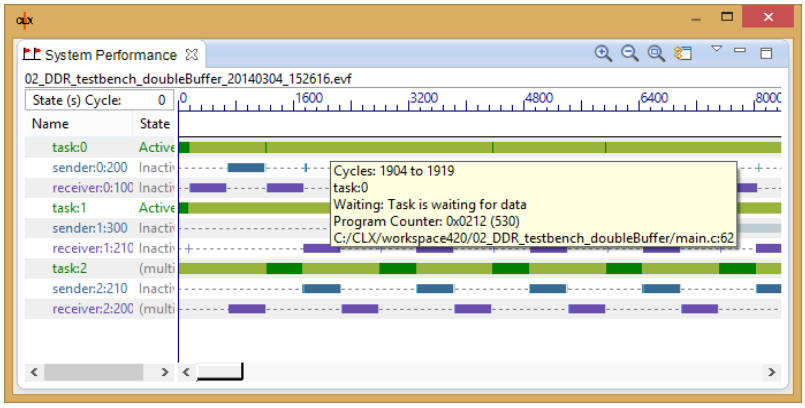
To port existing C code to the HyperX processor, high performance user kernels are compiled to the individual PEs. This is simplified by a number of features in the hxISDE. The MPI-based API functions allow the user to choose the communication method desired at compile time, or let the method be determined based on global optimization. This makes it easy to re-use existing code and focus on getting the best performance from the critical kernels, avoiding time consuming low level detail.

The hxISDE includes features like the event viewer and the task graph to aid the user in understanding the overall relationships between concurrent tasks and the causes of any performance bottlenecks. These graphical tools leverage the knowledge and talent of the designer to enable application performance optimization. The hxISDE image below shows a design currently being debugged.



Task and MPI-based data transfer visualization

The system performance tool on the right shows the cycle by cycle activity of all tasks and data send/receives in the system. Simply placing the cursor over a part of the activity graph provides details such as cycle count, program counter, and run status. By visualizing the activity of many concurrent processing cores, the user can make adjustments and quickly see the effects. The performance tool is linked to the source code viewer, so a mouse click immediately brings the user to the C code area of interest.



System Performance tool shows task activity

Complete multi-context analysis

The hxISDE provides true multi-context visibility in all of the different tools and views, including the source level display. This is especially important in supporting a many-core device that provides full support for parallel execution, since the same function may be at different points of execution in different cores. All references to a particular task and its status, program counter, full register set, and memory contents are clearly represented in the hxISDE.

The hxISDE debug session to the right shows the source code and breakpoints set in 4 independent tasks of the same source code which are run on different PEs.

Cycle-accurate simulation and debug

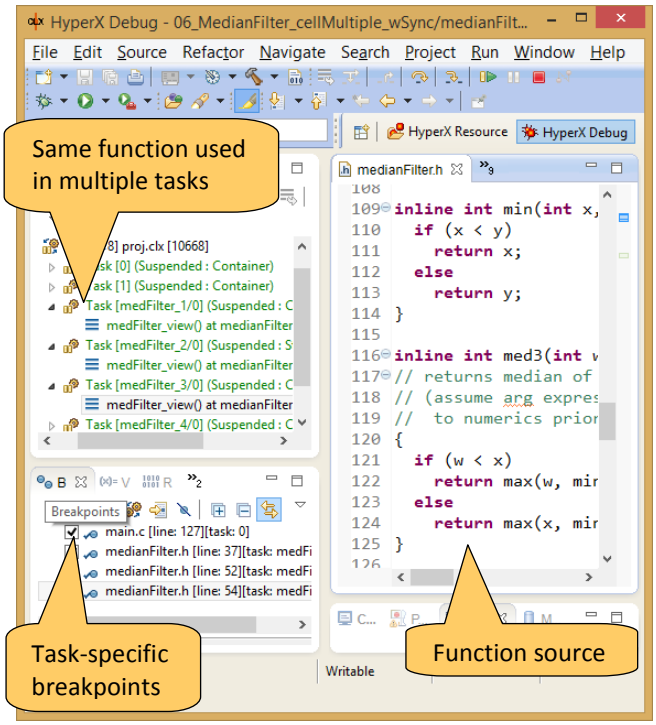
The simulation environment is cycle accurate for the entire system, including the PEs, on-chip network and the external IO interfaces. Multiple hx3100 devices can be simulated within the same environment, so system verification is greatly simplified. A rich set of simulation-control commands includes instruction and cycle mode stepping, and multiple breakpoint types. To help the user get straight to a scenario of interest, both functional and event breakpoints support a variety of conditions such as variable equations and ignore-counts. A configuration manager maintains all the detailed settings for multiple debugging sessions for later recall.

Consistent hxISDE through Hardware Debug

The same run and debug environment of the hxISDE is leveraged when the application code is run in the HyperX Hardware Application Development System (hxHADS). This fully integrated, modular environment supports multi-chip systems and a wide variety of interface standards. With hxHADS, applications are brought up and running far faster than possible with a custom board of FPGAs and processors. A host GPP is also included, and the host code can be debugged along with code running in the hx3100 devices.

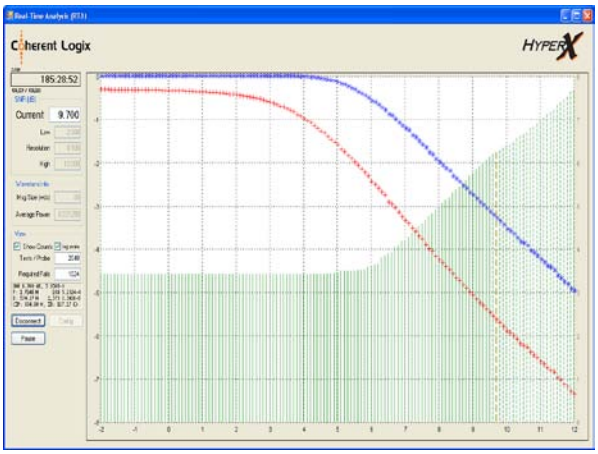
Real Time Analysis (RTA) for System Verification

For full verification, the hxHADS makes it easy to run applications like radio, DSP, and image processing for many millions of cycles. The RTA feature allows observability of internal nodes or registers in the hx3100 to be observed without affecting system operation or slowing down processor execution. This makes it possible to run interactive system tests that change based on internal information, automating tests and analysis.



Multi-context visibility and control

hxHADS development system



Channel BER analysis with RTA

HyperX Technology for your application

The hxISDE leverages existing standards to offer a low risk, field proven implementation path for high performance embedded systems. This approach brings faster time to market, higher revenue, greater flexibility, and lower total cost of ownership. To bring these benefits to your applications, ask us about our free training.

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Coherent Logix™
Enabling Low Power Software Defined Systems