ARTICLE – IP Cores

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Machine vision camera suppliers reduce time to market with transport layer IP Cores

The core competency of engineers designing machine vision cameras and systems is usually configuring the core camera features to provide the best possible image while meeting size, weight, power budget and other requirements. But they also have to devote considerable time and effort to successfully streaming the image from the camera to the host. Leading edge vision transport layer standards such as GigE Vision, USB3 Vision and CoaXPress (CXP) are complex and are evolving, so several months of work by experienced protocol engineers is typically required to design the interface.

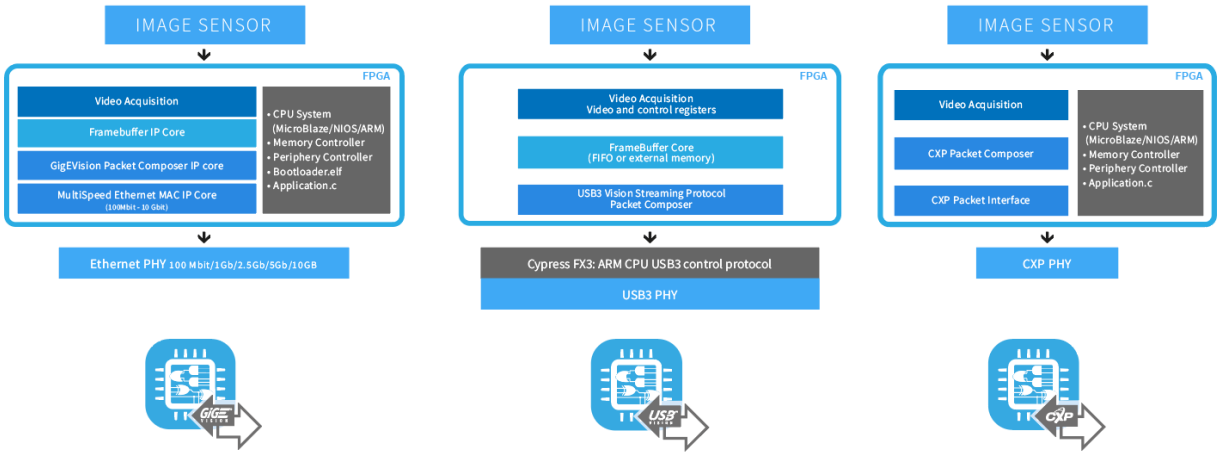
A number of manufacturers of leading-edge machine vision cameras, such as Ozray (formerly NIP), Crevis and Sick are addressing this challenge by purchasing transport layer interfaces in the form of intellectual property (IP) which is provided ready to incorporate into field programmable gate arrays (FPGAs) along with other camera features. “Use of IP Cores enables us to develop more cameras at the same time while reducing time to market,” said Keith Ahn, Executive Director and Chief Technology Officer for camera provider Ozray, Inc., Yongin-si, Korea. “The biggest advantage of using IP cores is that we can create a reliable standard transmission interface in a fraction of the time previously required,” said June Hwang, Chief Executive Officer of Crevis Co., a machine vision company also located in Yongin-si, Korea.

A decade ago, Camera Link was the most widely used machine vision transport layer interface. The streaming part of Camera Link was well defined, but the control path was not specified, so every camera implemented its own configuration protocol, requiring individual tweaks on host side to fully support the camera. Fast forward to today and machine vision communications between the camera and host computer has been largely standardized, primarily using CXP, GigE and USB interfaces. The new vision standards are more complex and require tighter timing margins than earlier generations. Further complications are provided by the fact that the standards themselves are evolving, requiring review of the standard and sometimes an upgrade of the transport layer implementation.
The emergence of machine vision transport layer IP cores reduces the time required to develop camera-host interfaces. For example, Sensor to Image (S2I), a unit of Euresys, a leading frame

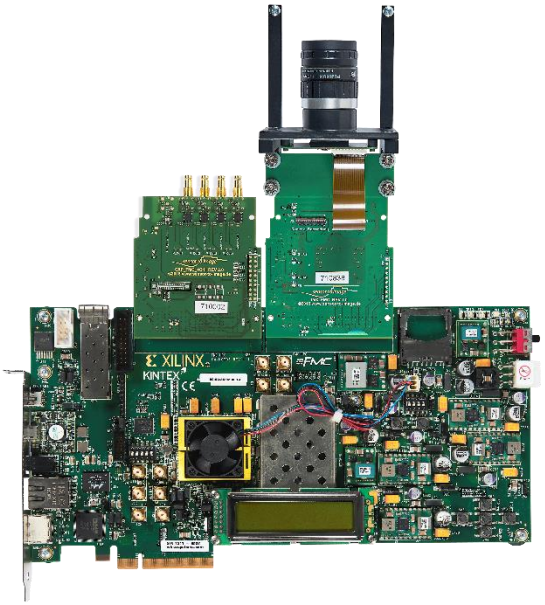
MVDK evaluation board with MIPI CSI-2 sensor and CXP interface board

grabber supplier, provides IP cores that meet the latest CXP, GigE Vision and USB3 Vision interface standards. These IP cores secure the interoperability of the camera and host while ensuring compliance with the latest version of the interface layer.

S2I's Vision Standard IP Cores solutions are delivered as a working reference design along with FPGA IP cores that have been fully tested against a wide range of popular frame grabbers and image acquisition libraries. The IP cores are compact, leaving plenty of room for additional vision functionality.



They are compatible with Xilinx 7 and newer and Intel/Altera Cyclone V and more recent devices.



Xilinx Kintex 7 evaluation board with CXP and IMX Pregius interface boards

Intel Cyclone 10 evaluation board with CXP interface board

The top-level design, consisting of the interface between external hardware such as the image sensor and transport layer PHY, is delivered as VHDL source code that can be adapted to

custom hardware beyond the leading FPGA platforms supported by IP cores. The Video Acquisition Module of the reference design simulates a camera with a test pattern generator. This module is delivered as VHDL source code which is replaced by a sensor interface and pixel processing logic in the camera design. An FPGA integrated CPU (either MicroBlaze, NIOS or ARM) is used for several non-time-critical control and configuration tasks on the Vision Standard IP Cores. This software is written in C and can be extended by the customer.

“By reusing IP cores, machine vision companies can focus on how to make the best image while maintaining full freedom to use any hardware needed to meet size, weight and power budget issues,” said Jean Caron, Vice President Sales and Support, EMEA for Euresys. “We work closely with the CoaXPress, USB3 Vision and GigE Vision committees to ensure that our IP cores comply with the latest revisions of the standards,” said Matthias Schaffland, IP Product Specialist at S2I. S2I has recently introduced an IMX Pregius IP core providing an interface to Sony Pregius Sub-LVDS image sensors. The company will also soon introduce an interface to MIPI sensors primarily used in embedded vision systems and mobile devices. S2I offers a volume license best suited for companies with a large product line as well as a single-piece license which is the best option for companies with smaller lines. Training and support are offered with either licensing arrangement.

Ozray is a machine vision camera supplier that has implemented IP cores in its Pollux and Pamina area and line scan cameras and its Deneb thermal camera. Ahn said that in-house development of CXP and GigE transport layer interfaces would have been considerably more expensive than purchasing IP. “By purchasing IP cores, we can focus internal engineering resources on image processing and controlling sensor functions to a degree that wasn’t possible in the past when so many resources were devoted to the camera-host interface,” Ahn said. “We are also now able to address new markets by expanding our interface offerings from Camera Link alone in the past to now offering CXP and GigE as well. We are 100% satisfied with the IP cores and services provided by S2I.”

Crevis is a leading supplier of machine vision cameras and industrial controllers. Hwang said that in the past it took a considerable amount of engineering manpower to develop the internal transmission logic, device drivers and Tx/Rx library for transport layer interfaces for its area scan cameras. “Now we purchase IP cores for GigE, CXP and USB interfaces from S2I while our engineers focus on developing sensor interface and camera functionality,” Hwang said. “S2I provides the reference design, training and technical support. This approach makes it possible to develop a reliable standard transmission interface in a fraction of the time required in the past. By incorporating IP cores into an FPGA that replaces many other parts, we have also reduced the size and manufacturing cost of our cameras.”

Sick's Ranger 3 3D streaming camera offers a greater number of 3D profiles per second in combination with a large height range and high image quality. "Previous generations of the Ranger 3 used a proprietary Gigabit Ethernet interface in order to provide capabilities that could not be delivered by following the standard," said Mattias Johannesson, Senior Expert, Software 3D Camera for SICK IVP AB. "When the standard grew to include the features we needed, we wanted to adopt it but didn't want to divert the engineering resources that would have been required to do the job internally. S2I offered a proven standard IP Core together with new custom modules to cover the extensions of the standard. We had very good communications with S2I throughout the implementation process including several face to face meetings. Our engineering team was able to focus on our imager and signal processor, making it possible to get the latest Ranger 3 version to market in considerably less time than would have been required if we had developed the interface in-house."

"IP Cores enable machine vision companies to build FPGA-based products using the GigE Vision, USB3 Vision, and CoaXPress standards, delivering the highest possible performance in a small footprint while minimizing development time," Schaffland concluded.

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